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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,025	07/22/2003	Woo Yeong Cho	8836-189 (ID12133-US)	8217

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EXAMINER	
NGUYEN, DANG T	
ART UNIT	**PAPER NUMBER**
2824	

DATE MAILED: 01/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/625,025	CHO, WOO YEONG	
	Examiner	Art Unit	
	Dang T Nguyen	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *19* is/are allowed.

6)☒ Claim(s) *1,5-10 and 14-18* is/are rejected.

7)☒ Claim(s) *2-4, 11-13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/03/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Search history*.

DETAILED ACTION

1. This office action is in response to applicant's amendment filed on 11/09/04. Claims 1 and 18 have been amended. Claim 19 has been added. Claims 1 – 19 are pending on this application. Claims 1, 10, and 19 are independent claims.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 5, 6, 8, and 9 are rejected under 35 U.S.C. 102(e) as being anticipated by Naji, U.S. Patent No. 6,418,046 B1 – filed Jan. 30, 2001.

Regarding independent claim 1, Fig. 1 of Naji discloses memory device comprising: a first memory array [left array memory 15] having a plurality of first memory cells [15's], wherein each one of the plurality of first memory cells [15] is arranged at an intersection of at least one of a plurality of wordlines, at least one of a plurality of bitlines, and at least one of a plurality of digit lines (See Figs. 2 – 4); a second memory array [right array memory 15] having a plurality of second memory cells [15's], wherein each one of the plurality of second memory cells is arranged at an intersection of at least one of the plurality of wordlines, at least one of a first bitline and a second bitline of

the plurality of bitlines, and at least one of the plurality of digit lines (Figs. 2 – 4); a current providing unit (Fig. 4 [42]) for providing a second current (output of 42) to a reference bitline (Fig. 4 [31]) in response to a reference voltage (Fig. 4 [VBIASREF]; and a sense amplifier (Fig. 4 [36]) for comparing a first current (Fig. 4 [30]) flowing through one of the plurality of bitlines with the second current (Fig. 4 [31]).

Regarding dependent claim 5, Naji discloses wherein the first and second memory cells are magnetic (Col. 2 lines 26 – 28).

Regarding dependent claim 6, Naji discloses wherein the first current (Fig. 4 [30]) is a target current (Col. 3 lines 18 – 20).

Regarding dependent claim 8, wherein the second current (Fig. 4 [31]) is a reference current (Col. 3 lines 18 – 20).

Regarding dependent claim 9, wherein the first current is compare to the second current to determined a logic state (Fig. 4 [Q; output of 36]) of a predetermined one of the plurality of the first memory cells (Fig. 4 [15]).

Claims 10, 14, 15, 17, and 18 are rejected under 35 U.S.C. 102(e) as being anticipated by Hidaka, U.S. Patent No. 6, 788,568 B2 – filed Jan. 18, 2002.

Regarding dependent claim 10, Fig. 38 of Hidaka discloses memory device comprising:

a plurality of first bitlines [BL1, BL2] and a plurality of second bitlines [/BL1,/BL2]; a first memory array (first and third rows of memory array 10) having a plurality of first memory cells [MC, DCB]; a second memory array (second and four rows of memory array 10) having a plurality of second memory cells [MC, DCB]; a current providing unit

[51, 52] for providing a second current to one of the plurality of second bitlines [/BL1,/BL2] in response to a reference voltage [Vref] and a sense amplifier [53] for comparing a first current [51, 52] flowing through one of the plurality of first bitlines [BL1, BL2] with the second current.

Regarding dependent claim 14, wherein the first memory cells and the second memory cells are magnetic (Col. 3 lines 39 – 40).

Regarding dependent claim 15, wherein the first current is a target current (this is intrinsic to Fig. 38 of Hidaka et al. since the comparator is comparing the currents between bit lines therefore each current of each bit line is either a target current or a reference current).

Regarding dependent claim 17, wherein the second current is a reference current (this is intrinsic to Fig. 38 of Hidaka et al. since the comparator is comparing the currents between bit lines therefore each current of each bit line is either a target current or a reference current).

Regarding dependent claim 18, wherein the first current is compare to the second current to determined a logic state [DOUT] of a predetermined one of the plurality of the first memory cells [MC, DPC].

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Naji, U.S. Patent No. 6,418,046 B1 in view of Nahas et al., U.S. Patent No. 6,600,690 B1 – filed Jun. 28, 2002.

Regarding dependent claim 7, Fig. 4 of Naji as applied to claim 1 above, fails to disclose wherein the second current is defined by the expression (I(H) + I(L))/2.

Fig. 1 of Nahas the current is defined by the expression (I(H) + I(L))/2 (Col. 4 lines 27-30).

Naji and Nahas are common subject for MRAM device. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporated Nahas's current expression into Naji second current for the purpose of establishing a saturated current level for the transistors (Col. 5 lines 41-42).

Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hidaka, US Patent No. 6,788, 568 B2 in view of Nahas et al., US Patent No. 6,600,690 B1 – filed Jun. 28, 2002.

Regarding dependent claim 16, Fig. 38 of Naji as applied to claim 10 above, fails to disclose wherein the second current is defined by the expression (I(H) + I(L))/2.

Fig. 1 of Nahas the current is defined by the expression (I(H) + I(L))/2 (Col. 4 lines 27-30).

Hidaka and Nahas are common subject for MRAM device. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was

made to incorporated Nahas's current expression into Hidaka second current for the purpose of establishing a saturated current level for the transistors (Col. 5 lines 41-42).

Allowable Subject Matter

4. Claims 2, 3, 4, 11, 12, and 13 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

With respect to claims 2 and 11, the prior art does not teach or suggest "wherein the current providing unit comprising: a first current mirror coupled to the first bitline; a second current mirror coupled to the second bitline; and a third current mirror for providing half of the sum of the current from the first bitline and the current from the second bitline to the sense amplifier".

With respect to claims 3 and 12, the prior art does not teach or suggest "wherein each one of the plurality of second memory cells set to a first logic state is coupled to the first bitline and each one of the plurality of second memory cells set to a second logic state is coupled to the second bitline".

With respect to claims 4 and 13, the prior art does not teach or suggest "a circuit for clamping down a voltage of a first data line through which the first current is transmitted, and a voltage of a second data line through which the second current is transmitted, to the reference voltage when one of the plurality of word lines of one of the plurality of first memory cells is enabled".

5. Claim 19 is allowed.

The following is an examiner's statement of reasons for allowance: in addition to other elements in the claim the prior art does not teach or suggest "a current providing unit comprising a first current mirror coupled to a second one of the plurality of bitlines; a second current mirror coupled to a third one of the plurality of bitlines; and a third current mirror for providing the reference current equal to half of the sum of a current from the first current mirror and a current from the second current mirror to the sense amplifier".

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

6. Applicant's arguments with respect to claims 1 and 10 have been considered but are moot in view of the new ground(s) of rejection.

Prior art

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Ooishi	Patent No. US 6,791,890	Date of Patent: Sep. 14, 2004
Tsen	Patent No. 5,936,906	Date of Patent: Aug. 10, 1999
Tanizaki	Patent No. US 6,707,737 B2	Date of Patent: Mar. 16, 2004

Contact Information

8. Any inquiry concerning this communication from the examiner should be directed to Dang Nguyen, who can be reached by telephone at (571) 272-1955. Normal contact times are M-F, 8:00 AM - 4:30 PM.

Upon an unsuccessful attempt to contact the examiner, the examiner's supervisor, Richard Elms, may be reached at (571) 272-1869.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist, whose telephone number is (703) 305-3900. The faxed phone number for organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the Status of an application may be obtained from the patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free) or EBC@uspto.gov.

Dang Nguyen 1/5/2005

VAN THU NGUYEN
PRIMARY EXAMINER